Amendments to the Specification:

Please replace the paragraph at page 9, line 7 to page 10, line 2 with the following amended paragraph:

Referring now to **Figure 2**, an 8-bit block **200** for a carry-skip adder according to embodiments of the present invention will now be further described. As shown in **Figure 2**, the block **200** illustrated in **Figure 2** includes ~~seven~~ eight bit stages **205, 207, 209, 211, 213** (five of which are shown). Each bit stage includes an exclusive NOR gate **224A, 224B, 224C, 224D, 224E** that receives the operands (X_i, Y_i). Each bit stage further includes an exclusive NOR gate **222A, 222B, 222C, 222D, 222E** that generates the respective sum outputs (S_i). The respective LSB bit stage **205** and next to lsb bit stage **207** include a single multiplexer **220A, 220B** generating a respective carry output (C_i) which becomes the carry input to the next most significant bit stage. Carry strength (CS_i) or bit associated propagation characteristic (bapc) signals which are independent of the block carry input (C_{in}) from another bit block of an adder including the bit block **200** are generated using the OR gates **230A, 230B, 230C, 230D**. Each of the carry strength signals (CS_i) are generated based on respective first and second operand bits (X_i, Y_i) input to the respective bit stages and, for all except the first carry strength signal (CS_1) based on the preceding stage carry strength signal. Thus, the illustrated circuit implements the equations for CS_{k+1} introduced above. Further note that the resulting sum bits for the bit stages **207, 209, 211, 213** are each generated based on the respective bit stage operand bits (X_i, Y_i) and the respective bit stage carry input (C_i). The bit stages **209, 211, 213** each include an additional multiplexer **226C, 226D, 226E,** thus allowing these respective bit stages to select either the carry input to the bit block (C_{in}) or a calculated carry output (C_i) to provide as the carry input (C_{i+1}) into the next most significant bit stage. The initial bapc (CS_1) is also independent of the carry input to the block (C_{in}) and is based solely on the operands (X_0, Y_0) input to the lsb bit stage **205**. More particularly, CS_1 is the exclusive NOR of the operands X_0, Y_0 input to the lsb bit stage **205**.